https://doi.org/10.30799/jnst.187.18040530 J. Nanosci. Tech. - Volume 4 Issue 5 (2018) 575–579

Share Your Innovations through JACS Directory

Journal of Nanoscience and Technology

Visit Journal at http://www.jacsdirectory.com/jnst

ISSN: 2455-0191

Design and Analysis of CMOS and CNTFET based Ternary Operators for Scrambling

Gudala Konica*, Sreenivasulu Mamilla

Department of Electronics and Communication Engineering, Gayatri Vidya Parishad College of Engineering (A), Affiliated to JNTUK, Visakhapatnam – 530 048, Andhra Pradesh, India.

ARTICLE DETAILS

Article history:
Received 17 November 2018
Accepted 03 December 2018
Available online 04 January 2019

Keywords:
CNTFET
Scrambling
Ternary Logic
Ternary Operator
MVL

ABSTRACT

As silicon technology scales down, it is a dominant choice to have high-performance digital circuits. As researchers investigated for high-performance digital circuits for future generations, Carbon Nanotube Field Effect Transistors (CNTFETs) is considered as the most promising technology due to their excellent current driving capability and proved to be an alternative to conventional CMOS technology. A CNTFET based energy efficient ternary operators are proposed for scrambling applications. The transistor-level implementations of operators namely Scrambling Operator1 (SOP1), Scrambling Operator2 (SOP2) and SUM operators are simulated with CMOS and CNTFET in 32 nm technology at 0.9 V supply voltage using Synopsys HSPICE. The performance metrics like Power, Delay and Power-delay product (PDP) are measured and a comparative analysis for CNTFET and CMOS technologies is carried out. The results demonstrate that CNTFET designs have better-optimized results in power, energy consumption, and reduced transistor count.

1. Introduction

Scrambling is widely used in digital communication systems consisting of transmitting and receiving terminals, and a transmission media. The main target is to encode digital signals by using a scrambler at the transmitter side and decode them by a descrambler at the receiver side. In today's VLSI design, interconnects complexity became a serious issue. MVL is an alternative to this solution [1]. Ternary logic surpasses binary in terms of higher computational speed since ternary digit (trit) has more information than a binary digit (bit). Now-a-days, ternary logic (or three-valued logic) has attracted due to its advantages over binary logic for designing digital systems. Simple and efficient design, less memory requirement, reduced interconnection complexity, and low product cost [2], reduction in chip area, and implementation of arithmetic and logic functions in a single IC are some of the advantages of MVL. Ternary logic is radix-3 number system which has three logic states, 0, 1 and 2 representing false, intermediate and true, respectively. Many ternary logic circuit models exist in the literature for CMOS technology but are not effective for present high-performance applications. Hence, a new technology (CNTFET) came into existence with better parametric results with low power, delay, and area. Over the past few decades, carbon nanotubes (CNTs) have drawn significant attention in the field of electronics, due to their unique structure and excellent physical properties. In this paper, the comparative analysis between CNTFET and CMOS designs are discussed.

Cryptography plays an important role in telecommunication systems. The general method used to scramble a data stream is the symmetric encryption where the original data stream called plaintext is combined with a keystream to generate an encrypted data, known as ciphertext at the transmitter side. Exclusive-OR (XOR) equivalent to modulo-2 addition is the operator used in binary logic to generate ciphertext.

$$\text{Plaintext} \oplus \text{keystream} = \text{Ciphertext} \quad (1)$$
$$\text{Ciphertext} \oplus \text{keystream} = \text{Plaintext} \quad (2)$$

While at the receiver side, the ciphertext is combined with the same key stream using the XOR operator to get plaintext back. All the data streams namely plaintext, keystream, and ciphertext are consequently a sequence of trits ∈{0,1,2}, (for example, 01221121). A general architecture for cryptography with encryption and decryption steps is shown in Fig. 1 for binary logic.

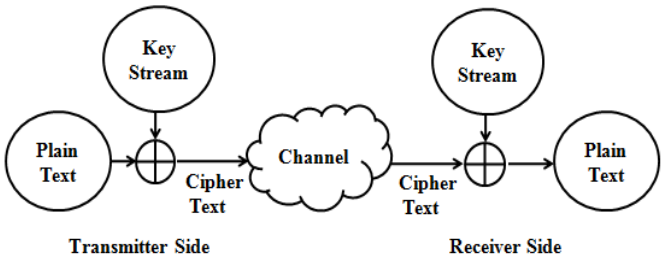

Fig. 1 A general architecture for encryption and decryption

Moreover, in ternary logic, the operator ⊕ represents mod-3 addition or SUM function in a ternary adder, follows the architecture shown in Fig. 2. The SUM operator is utilized twice to retrieve the original message sent by the sender as shown in Fig. 2. Because of more decoding steps, SUM is not an efficient ternary operator to use in cryptography.

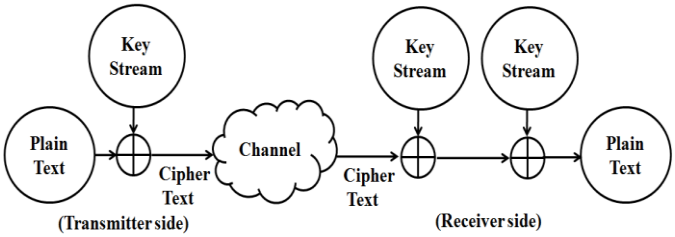

Fig. 2 Encryption and decryption steps for ternary SUM operator

Hence, two scrambling operators (SOP1 and SOP2) are designed in 32-nm Bulk CMOS technology [3] such that they follow the architecture shown in Fig. 1. The operators SOP1 and SOP2 have single encoding and decoding step. For better performance, the operators are proposed in 32-nm CNTFET Technology.

*Corresponding Author:konicaece@gmail.com(Gudala Konica)

https://doi.org/10.30799/jnst.187.18040530

2. Ternary Operators in CNTFET Technology

CNTFET is a three terminal device like MOS, where the semiconducting channel between the two contacts called Source and Drain consists of a Nanotube. Because of high electron mobility, high mechanical and thermal stability of CNTs, CNTFETs are being considered as one of the most promising ones. The representation of voltage levels in unbalanced ternary logic is 0, $V_{dd}/2$, V_{dd}, for logic values 0, 1, 2, respectively. There are three representations of ternary inverter namely Negative (-), Positive (+) and Standard and its truth table is mentioned [4]. The positive (negative) ternary inverter takes a path to V_{dd} (Gnd) when the input is logic '1' where, Vdd and Gnd represent logic '2' and '0', respectively. Let p, q and C be the plaintext, keystream, and Ciphertext which consists of trits ∈{0,1,2}. The SOP1 and SOP2 operators are designed such that they satisfy Eqs. (3) and (4). Moreover, the same is not possible for SUM Eq.(5) but it can be applied to cryptography by using operator three times Eq.(6) as shown in Table 1. The truth table for a two input ternary function (p, q) for SUM, SOP1 and SOP2 are summarized in Table 2 [3].

$$SOP1(p,q) = C \quad and \quad SOP1\,(C,q) = p \tag{3}$$
$$SOP2(p,q) = C \quad and \quad SOP2\,(C,q) = p \tag{4}$$
$$SUM(p,q) = C \quad and \quad SUM\,(C,q) \neq p \tag{5}$$
$$SUM(p,q) = C \quad and \quad SUM\big(\,(SUM\,(C,q)),q\,\big) = p \tag{6}$$

Table 1 Truth table for SUM in Cryptography

p	q	$SUM(p,q)$ (C)	$SUM(C,q)$ (x)	$SUM(x,q)$ (p)
0	0	0	0	0
0	1	1	2	0
0	2	2	1	0
1	0	1	1	1
1	1	2	0	1
1	2	0	2	1
2	0	2	2	2
2	1	0	1	2
2	2	1	0	2

Table 2 Truth table for SUM, SOP1, and SOP2 operators

p	q	SUM	$SOP1$	$SOP2$
0	0	0	0	1
0	1	1	2	1
0	2	2	1	2
1	0	1	1	0
1	1	2	1	0
1	2	0	0	1
2	0	2	2	2
2	1	0	0	2
2	2	1	2	0

2.1 Transistor-Level Implementation of Ternary Operators

There are several ternary adder designs exists in literature survey [5-8]. The method of ternary circuitry in [7] is used to implement ternary operators in transistor level where the average of $(\overline{\overline{Out}+})$ and $(\overline{\overline{Out}-})$ generates the standard ternary function 'Out'. The sub-circuits has CMOS binary structures consists of PMOS transistors in Pull-up and NMOS transistors in Pull-down networks that generate the mid-outputs values at $\overline{Out}+$ and $\overline{Out}$-.

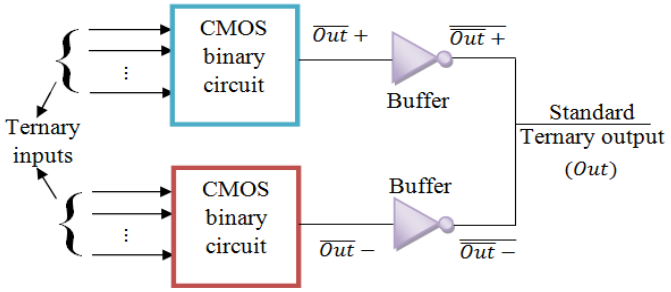

Fig. 3 Method of ternary circuitry used to design CNTFET [7]

As CNTFET has an excellent current driving capability, a single inverting buffer is enough to strengthen the signal and converts mid-outputs into $(\overline{\overline{Out}+})$ and $(\overline{\overline{Out}-})$. Then, the voltage division takes place to generate the standard ternary function Out as shown in Eq.(7). The fewer times the voltage division, less power dissipates [7]. The method of ternary circuitry used to design CNTFET based ternary operators is shown in Fig. 3.

$$Out = \frac{(\overline{\overline{Out}+}) + (\overline{\overline{Out}-})}{2} \tag{7}$$

The transistor-level implementation of CNTFET based SUM, SOP1, and SOP2 are depicted in Figs. 6-8. The ternary inputs in Fig. 3 can be Positive Ternary Inverters (PTI) and Negative Ternary Inverters (NTI), used to complement the input variables (p, q). Two Logic One Detectors [8] are also needed to check whether the input variables p, q are '1' or not.

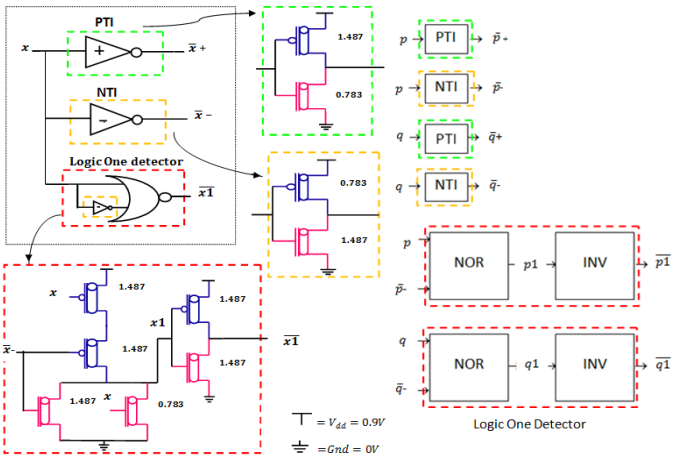

Fig. 4 Transistor-level and Gate-level implementations of PTI, NTI and Logic One Detector

The gate-level and transistor-level structure for PTI, NTI, and logic one detectors are shown in Fig. 4. Each transistor is represented with the diameter of CNT (in nm). For diameters 0.783, 1.487, and 1.096, the chirality numbers are (10, 0), (19, 0), and (14, 0), and corresponding threshold voltages are 0.549 V, 0.289 V, and 0.392 V, respectively. The mathematical formula for calculating the diameter of CNT and the threshold voltage is shown in Eqs. (8) and (9), respectively [6, 7].

$$D_{CNT} = a_0 \frac{\sqrt{3}}{\pi} * \sqrt{n^2 + m^2 + nm} = 0.0783 * \sqrt{n^2 + m^2 + nm} \tag{8}$$
$$V_{th} = \frac{E_g}{2e} = \frac{a_0\, V_\pi}{e\, D_{CNT}} \approx \frac{0.43}{D_{CNT}(nm)} \tag{9}$$
$$(\overline{SOP1}+)^2\,(pullup) = p^0q^0 + p^0q^2 + p^1q^0 + p^1q^1 + p^1q^2 + p^2q^1 \tag{10}$$
$$= p^0(q^0 + q^2) + p^1(q^0 + q^1 + q^2) + p^2q^1 = p^0(q^0 + q^2) + p^1 + p^2q^1 \tag{10.1}$$
$$(\overline{SOP1}+)^0\,(pulldown) = p^0q^1 + p^2q^0 + sp^2q^2 = p^0q^1 + p^2(q^0 + q^2) \tag{11}$$
$$(\overline{SOP1}-)^2\,(pullup) = p^0q^0 + p^1q^2 + p^2q^1 \tag{12}$$
$$(\overline{SOP1}-)^0(pulldown) = p^0q^1 + p^0q^2 + p^1q^0 + p^1q^1 + p^2q^0 + p^2q^2 \tag{13}$$
$$= p^0(q^1 + q^2) + p^1(q^0 + q^1) + p^2(q^0 + q^2) = p^0q^{1|2} + p^1q^{0|1} + p^2(q^0 + q^2) \tag{13.1}$$
$$(\overline{SOP2}+)^2(pullup) = p^0q^0 + p^0q^1 + p^1q^0 + p^1q^1 + p^1q^2 + p^2q^2 \tag{14}$$
$$= p^0(q^0 + q^1) + p^1(q^0 + q^1 + q^2) + p^2q^2 = p^0q^{0|1} + p^1 + p^2q^2 \tag{14.1}$$
$$(\overline{SOP2}+)^0\,(pulldown) = p^0q^2 + p^2q^0 + p^2q^1 \tag{15}$$
$$= p^0q^2 + p^2(q^0 + q^1) = p^0q^2 + p^2q^{0|1} \tag{15.1}$$
$$(\overline{SOP2}-)^2\,(pullup) = p^1q^0 + p^1q^1 + p^2q^2 = p^1q^{0|1} + p^2q^2 \tag{16}$$
$$(\overline{SOP2}-)^0\,(pulldown) = p^0q^0 + p^0q^1 + p^0q^2 + p^1q^2 + p^2q^0 + p^2q^1 \tag{17}$$
$$= p^0(q^0 + q^1 + q^2) + p^1q^2 + p^2(q^0 + q^1) = p^0 + p^1q^2 + p^2q^{0|1} \tag{17.1}$$
$$(\overline{SUM}+)^2\,(pullup) = p^0q^0 + p^0q^1 + p^1q^0 + p^1q^2 + p^2q^1 + p^2q^2 \tag{18}$$
$$= p^0(q^0 + q^1) + p^1(q^0 + q^2) + p^2(q^1 + q^2) = p^0q^{0|1} + p^1(q^0 + q^2) + p^2q^{1|2} \tag{18.1}$$
$$(\overline{SUM}+)^0\,(pulldown) = p^0q^2 + p^1q^1 + p^2q^0 \tag{19}$$
$$(\overline{SUM}-)^2\,(pullup) = p^0q^0 + p^1q^2 + p^2q^1 \tag{20}$$
$$(\overline{SUM}-)^0\,(pulldown) = p^0q^1 + p^0q^2 + p^1q^0 + p^1q^1 + p^2q^0 + p^2q^2 \tag{21}$$
$$= p^0(q^1 + q^2) + p^1(q^0 + q^1) + p^2(q^0 + q^2) = p^0q^{1|2} + p^1q^{0|1} + p^2(q^0 + q^2) \tag{21.1}$$

The (n, m) indices are chirality numbers that indicate a vector when a graphene sheet is rolled to form a CNT. The threshold voltage (V_{th}) of the intrinsic CNT channel is approximately equivalent to half the energy band gap (E_g) of the CNT. By varying the diameter of CNT (D_{CNT}), the Vth can be altered as given in Eq.(9), where V_π (= 3.033 eV) is the carbon π-π bond energy in eV and e (= $1.6x10^{-19}$c) is the unit electron charge.

The ternary operators are constructed using ternary algebraic expressions from Eqs. (10-24) are needed. The input variables p and q have logic values 0, 1 and 2 can be represented by superscripts. For example, p^0 indicates the value of p is 0, and $p^{1|2}$ indicates the value of p is

https://doi.org/10.30799/jnst.187.18040530

Cite this Article as: Gudala Konica, Sreenivasulu Mamilla, Design and analysis of CMOS and CNTFET based ternary operators for scrambling, J. Nanosci. Tech. 4(5) (2018) 575–579.

1 or 2. The mid-outputs (for example, $(\overline{SUM}+)$ and $(\overline{SUM}-)$ are binary functions results in logic 2 (logic 0), whenever they take a path to the power supply (ground), through a pull-up network (pull-down network).

The ternary expressions are simplified by unifying the literals wherever possible. The terms (p^0+p^1) and (p^1+p^2) can be replaced by a single transistor $p^{0|1}$ and $p^{1|2}$, respectively. The same unification is not possible for the term (p^0+p^2). For $t^{0|1}$ $(t^{1|2})$, $t \in \{p,q\}$, is represented by a pCNTFET (nCNTFET) whose threshold voltage is set properly so that the transistor switches off (switches on) above $2V_{dd}/3$ ($V_{dd}/3$). The ternary expressions are shown in Eqs. (10-21) for SOP1, SOP2 and SUM operators.

For example, in Eq. (18), $(\overline{SUM}+)^2$ represents that the value of $(\overline{SUM}+)$ is '2'. The ternary expression for $(\overline{SUM}+)^2$ takes the combination of all minterms (p, q), whenever the mid-output, $(\overline{SUM}+)$ value is '2' as shown in Table3. The block diagram representation of SUM operator is shown in Fig. 5.

Table 3 Truth table of SUM with its mid output values

p	q	SUM	$\overline{SUM}+$	$\overline{SUM}-$
0	0	0	2	2
0	1	1	2	0
0	2	2	0	0
1	0	1	2	0
1	1	2	0	0
1	2	0	2	2
2	0	2	0	0
2	1	0	2	2
2	2	1	2	0

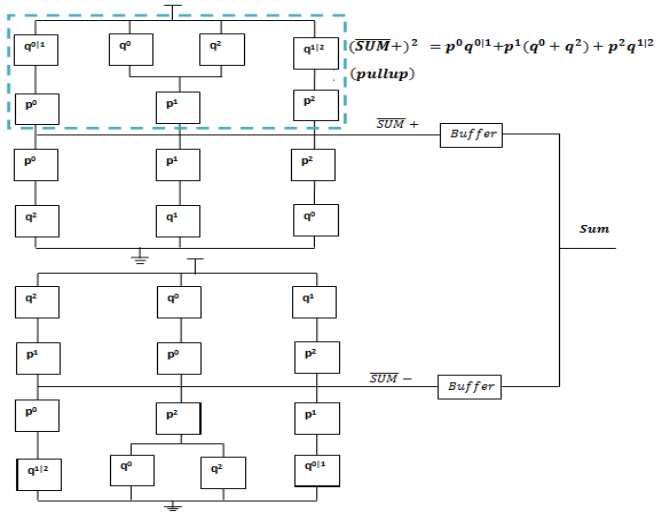

Fig. 5 Block diagram representation of SUM operator

Table 4 Representation of ternary inputs with CNTFET transistors

p (or) q	pCNTFET		nCNTFET	
p^0	p	0.783	$\bar{p}$-	1.487
p^1	$\bar{p}$1	1.487	p1	1.487
p^2	$\bar{p}$+	1.487	p	0.783
$p^{0\|1}$	p	1.487	$\bar{p}$+	1.487
$p^{1\|2}$	$\bar{p}$-	1.487	p	1.487

The ternary inputs $p^0, p^1, p^2, p^{0|1}, p^{1|2}$ can be represented with a CNTFET transistor with its diameter specified as in Table 4. Therefore, by replacing inputs with transistors in Fig. 5, the final ternary circuitry for transistor-level implementation of SUM operator is obtained as shown in Fig. 6.

In Fig. 6, the SUM operator is designed with 52 transistors and the numbers highlighted with red color represents the active paths of transistors. For example, the transistors marked with 1 connect the $(\overline{SUM}+)$ node to the power supply (V_{dd}) when (p,q) = (0, 0) and (0, 1). The transistors marked with 13, 16 connects the $(\overline{SUM}-)$ node to the ground terminal when (p,q) = (2, 0). The transistors marked with 3, 8 connects the $(\overline{SUM}+)$ node to the Vdd when (p, q) = (1, 2). Similarly, for all other input combination of minterms, depending upon the active paths the $(\overline{SUM}+)$ and $(\overline{SUM}-)$ nodes connect to V_{dd} or Gnd and assigns value 2 or 0, respectively. The truth table for SUM is shown in Table 5 with its mid-outputs and its path numbers.

Similarly, the transistor-level implementation of SOP1 and SOP2 is designed with 50 and 44 transistors, respectively as shown in Figs. 7 and 8. The truth tables for SOP1 and SOP2 with its mid-output values and its active transistor path numbers are shown in Tables 7 and 8.

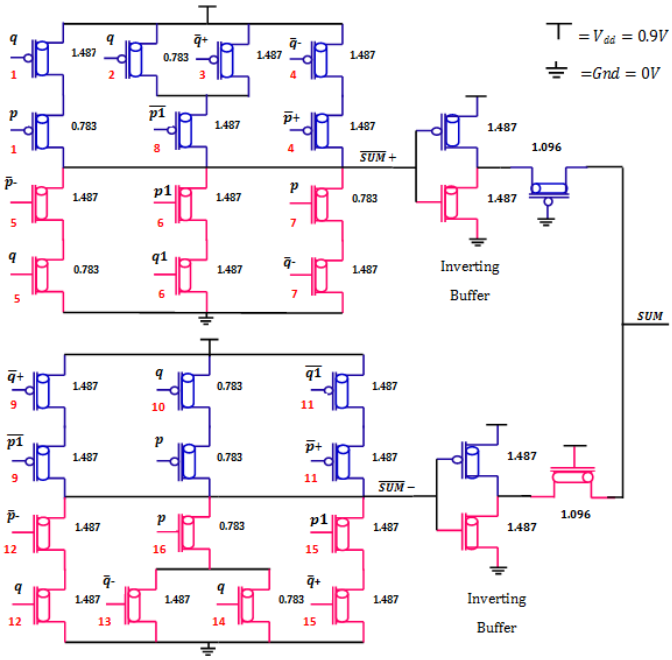

Fig. 6 Transistor-level implementation of CNTFET based SUM operator

Table 5 Truth table for SUM with mid-output values and active path numbers

p	q	$\bar{p}+$	$\bar{p}-$	$p1$	$\overline{p1}$	$\bar{q}+$	$\bar{q}-$	$q1$	$\overline{q1}$	SUM	$\overline{SUM}+$ and its $Path(s)$		$\overline{SUM}-$ and its $Path(s)$	
0	0	2	2	0	2	2	2	0	2	0	2	1	2	10
0	1	2	2	0	2	2	0	2	0	1	2	1	0	12
0	2	2	2	0	2	0	0	0	2	2	0	5	0	12
1	0	2	0	2	0	2	2	0	2	1	2	2,8	0	15
1	1	2	0	2	0	2	0	2	0	2	0	6	0	15
1	2	2	0	2	0	0	0	0	2	0	2	3,8	2	9
2	0	0	0	0	2	2	2	0	2	2	0	7	0	13, 16
2	1	0	0	0	2	2	0	2	0	0	2	4	2	11
2	2	0	0	0	2	0	0	0	2	1	2	4	0	14, 16

Table 6 CMOS Model parameters

Parameter	Description	Value
L_{ch}	Channel Length	32 nm
L_{eff}	Effective gate channel length	12.6 nm
R_{dsw}	Source and drain resistance per unit channel width	150Ω-μm
T_{ox}	Gate oxide thickness	1 nm
C_{gbo}	The gate-to-bulk overlap capacitance per unit channel length	25.6 pF/m
C_{gdl}/C_{gsl}	The overlap capacitance between gate and lightly doped drain/source region	265.3 pF/m

Table 7 Truth table for SOP2 with mid-output values and active path numbers

p	q	$\bar{p}+$	$\bar{p}-$	$p1$	$\overline{p1}$	$\bar{q}+$	$\bar{q}-$	$q1$	$\overline{q1}$	$SOP1$	$\overline{SOP1}+$ and its $Path(s)$		$\overline{SOP1}-$ and its $Path(s)$	
0	0	2	2	0	2	2	2	0	2	0	2	2,8	2	9
0	1	2	2	0	2	2	0	2	0	2	0	5	0	12
0	2	2	2	0	2	0	0	0	2	1	2	3,8	0	12
1	0	2	0	2	0	2	2	0	2	1	2	1	0	15
1	1	2	0	2	0	2	0	2	0	1	2	1	0	15
1	2	2	0	2	0	0	0	0	2	0	2	1	2	10
2	0	0	0	0	2	2	2	0	2	2	0	6, 17	0	13, 16
2	1	0	0	0	2	2	0	2	0	0	2	4	2	11
2	2	0	0	0	2	0	0	0	2	2	0	7, 17	0	14, 16

https://doi.org/10.30799/jnst.187.18040530

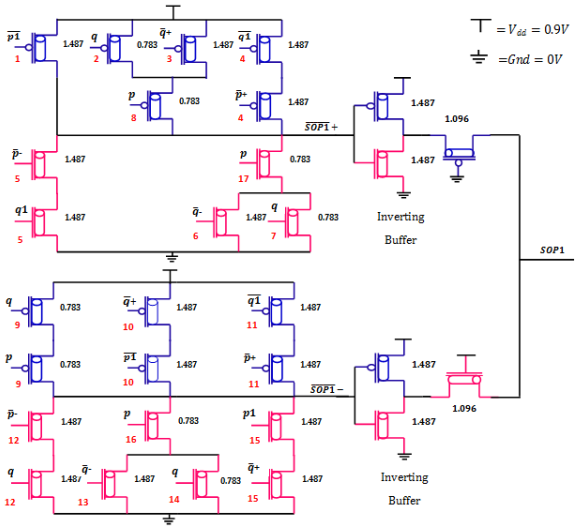

Fig. 7 Transistor-level implementation of CNTFET based SOP1

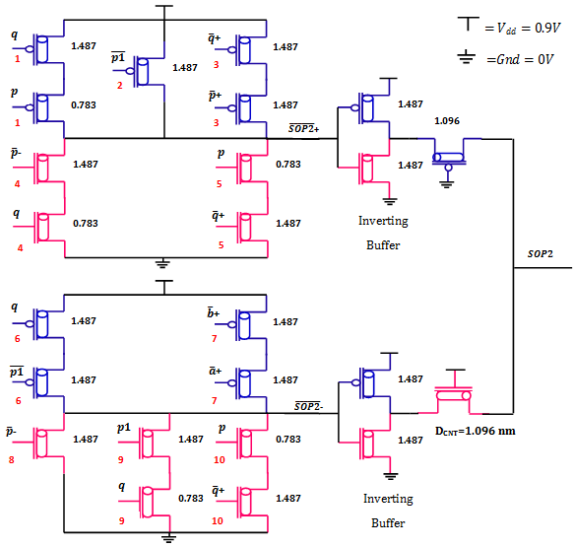

Fig. 8 Transistor-level implementation of CNTFET based SOP2

Table 8 Truth table for SOP2 with mid-output values and active path numbers

p	q	$\bar{p}+$	$\bar{p}-$	$p1$	$\overline{p1}$	$\bar{q}+$	$\bar{q}-$	$q1$	$\overline{q1}$	$SOP2$	$\overline{SOP2}+$ and its $Path(s)$		$\overline{SOP2}-$ and its $Path(s)$	
0	0	2	2	0	2	2	2	0	2	1	2	1	0	8
0	1	2	2	0	2	2	0	2	0	1	2	1	0	8
0	2	2	2	0	2	0	0	0	2	0	0	4	0	8
1	0	2	0	2	0	2	2	0	2	2	2	2	2	6
1	1	2	0	2	0	2	0	2	0	2	2	2	2	6
1	2	2	0	2	0	0	0	0	2	1	2	2	0	9
2	0	0	0	0	2	2	2	0	2	0	0	5	0	10
2	1	0	0	0	2	2	0	2	0	0	0	5	0	10
2	2	0	0	0	2	0	0	0	2	2	2	3	2	7

3. Results and Discussion

All CNTFET circuits are simulated with CNFET compact model [9]. The model parameters for CNTFET are provided [7]. The performance parameters are measured in Synopsys HSPICE tool at 0.9 V power supply. The average power for all possible transitions is measured for all circuits. For measuring delay, the fan-out of 4 ternary inverters (TFO4) is considered as output load. The complete input pattern that covers all possible transitions 0 to 1, 1 to 2, 0 to 2, 2 to 1, 1 to 0 and 2 to 0 is fed to the circuit and the maximum is reported as delay value. For a two-input function (p, q) with 9 minterms, there are 9*8=72 possible transitions since every single minterm can change into the eight other minterms. For example, the minterm 00 can change into 01, 02, 10, 11, 12, 20, 21, 22. The Power-delay product is the balance between maximum delay and average power calculated (22).

$$Power - Delay\ Product\ (PDP) = Average\ power * Max.Delay \quad (22)$$

To provide a comparison between CMOS and CNTFET technologies, the transistor-level implementation of ternary operators in CMOS [3] are simulated with 32 nm bulk CMOS technology at 0.9 V supply voltage. The parameters given in table6 are utilized to define model files in Predictive technology model [10] for simulation. As the current driving capability of CMOS is weaker, Buffers are supplemented to drive the current. For CNTFET, two buffers are eliminated due to its high current driving capability which leads to a reduction in transistors. The transient response for SOP1 in CMOS and CNTFET is shown in Figs. 9 and 10, with 58 and 50 transistors, respectively.

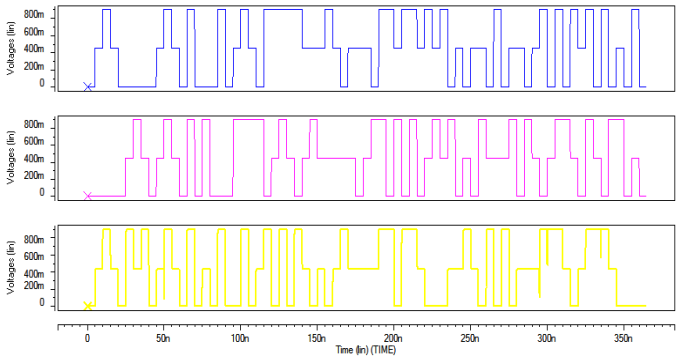

Fig. 9 Transient response of SOP1 in CMOS technology

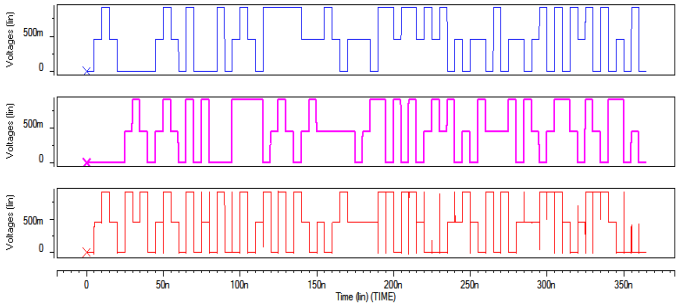

Fig. 10 Transient response of SOP1 in CNTFET technology

The transient response for SOP2 in both technologies is shown in Figs. 11 and 12. SOP2 in CMOS [3] design has 52 transistors whereas CNTFET design for SOP2 has 44 transistors. Figs. 13 and 14 show the transient response of SUM in CMOS and CNTFET designs that has 60 and 52 transistors, respectively.

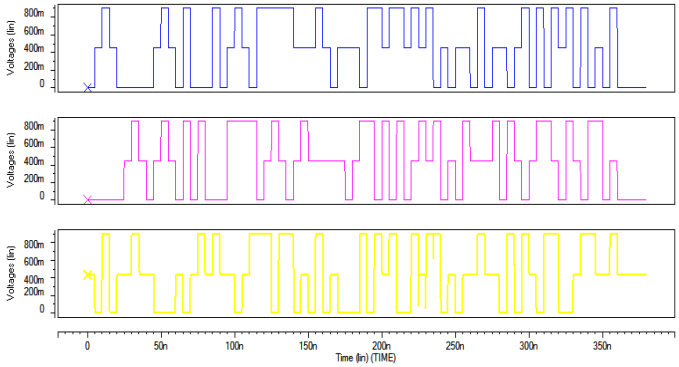

Fig. 11 Transient response of SOP2 in CMOS technology

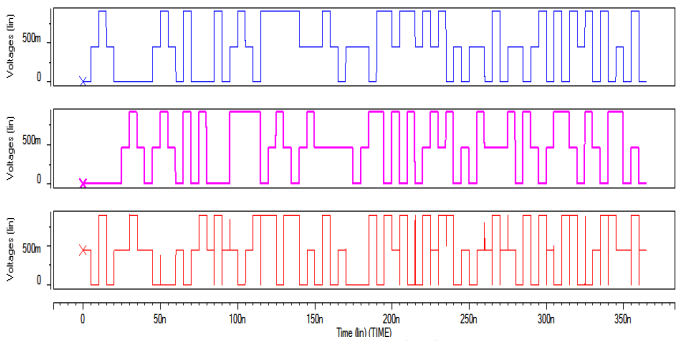

Fig. 12 Transient response of SOP2 in CNTFET technology

https://doi.org/10.30799/jnst.187.18040530

Cite this Article as: Gudala Konica, Sreenivasulu Mamilla, Design and analysis of CMOS and CNTFET based ternary operators for scrambling, J. Nanosci. Tech. 4(5) (2018) 575–579.

The average power, delay, PDP, transistor count, total cell width of all operators are compared for CMOS and CNTFET designs as reported in Table 9. By comparing each ternary operator designed with CMOS and CNTFET, the CNTFET designs have better performance. For operators SUM, SOP1 and SOP2, the CNTFET designs have lower power-delay product (PDP) than the operators designed in CMOS. The CNTFET based SOP2 has the least PDP and also it has the lower transistor count and lower cell width. Hence, CNTFET based SOP2 occupies less area in a chip. As it has lower PDP, it is a high-energy efficient ternary operator for scrambling. The total cell width of CNTFET circuit is calculated by considering the sum of each transistor width Eq.(24). The transistor width is calculated by Eq.(23) [7] where W_{min} is the minimum width of the gate and N is the number of nanotubes placed under the transistor gate ($N = 3$). By considering Eq.(23), the cell width for each transistor is 60nm. The SOP2 design has the least cell width which intends to decrease in the area of a chip.

$$W_g = Min(W_{min}, N * Pitch) \quad (23)$$

$$Total\ cell\ width = \sum width\ of\ transistors\ (W_g) \quad (24)$$

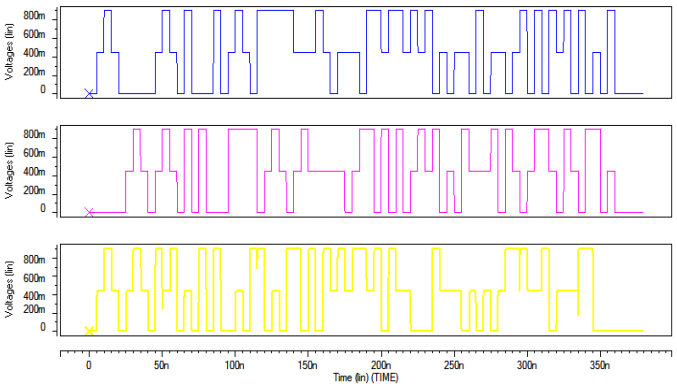

Fig. 13 Transient response of SUM in CMOS technology

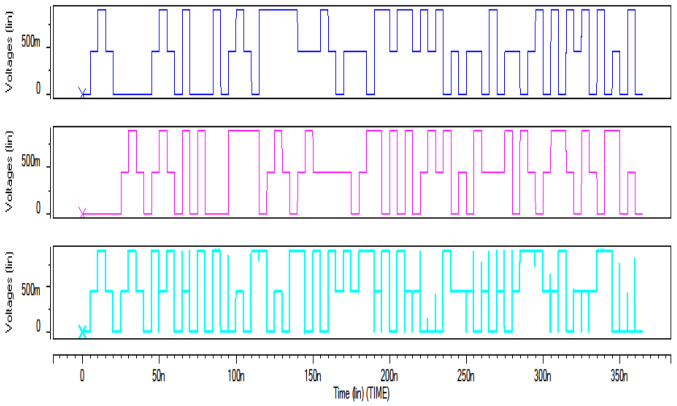

Fig. 14 Transient response of SUM in CNTFET technology

Table 9 Comparative analysis of ternary operators in CMOS and CNTFET Designs

Operator	Design	Average Power (μw)	Maximum Delay (ns)	PDP (fJ)	Transistor Count	Total cell width (nm)
SUM	CMOS	1.9659	0.5680	1.1166	60	7900
	CNTFET	0.28458	0.046545	0.013245	52	3120
SOP1	CMOS	1.9457	0.4916	0.9565	58	7824
	CNTFET	0.28203	0.044469	0.012541	50	3000
SOP2	CMOS	1.8631	0.5016	0.9345	52	7232
	CNTFET	0.25039	0.046436	0.011627	44	2640

4. Conclusion

The transistor-level designs for CNTFET based Ternary operators, SOP1, SOP2, and SUM, have been proposed in this paper which optimizes the performance metrics with lower power consumption, lesser PDP, reduced transistor count and occupying least area in a chip. They can be used in digital coding in communication systems. A comparative analysis is performed for ternary operators designed with CMOS and CNTFET in 32 nm technology, to conclude the superior technology for ternary circuitry in scrambling applications. In comparison with CMOS, the proposed CNTFET based ternary operators benefit from low power consumption, reduced transistor count and less area. The performance is enhanced because of its excellent current driving capability. The results show that the Power delay product of CNTFETs is less when compared to CMOS designs. The transistor count is reduced from 52 in CMOS to 44 in CNTFET based SOP2. Hence, SOP2 consumes the least area in a chip. CNTFETs are more flexible in adjusting the threshold voltage of transistors by varying the diameter of CNT. This feature makes CNTFET highly appropriate for multi threshold voltage circuitry. The current driving capability of CNTFETs is higher than CMOS. Hence, CNTFETs are the most promising ones in designing the ternary operators for scrambling.

References

[1] E. Dubrova, Multiple-valued logic in VLSI: Challenges and opportunities, Proc. NORCHIP Conf. 1 (1999) 340-350.
[2] S.L. Hurst, Multiple-valued logic – its status and its future, IEEE Trans. Comput. C 33(2) (1984) 1160-1179.
[3] M.S. Daliri, R. Faghih Mirzaee, K. Navi, N. Bagherzadeh, High-performance ternary operators for scrambling, integration, VLSI Journal 59 (2017) 1-9.
[4] M.H. Moaiyeri, A. Doostaregan, K. Navi, Design of energy-efficient and robust ternary circuits for nanotechnology, IET Circ. Device. Syst. 5(4) (2011) 285-296.
[5] R.F. Mirzaee, M.H. Moaiyeri, M. Maleknejad, K. Navi, O. Hashemipour, Dramatically low-transistor-count high-speed ternary adders, IEEE 43rd Int. Symp.n Multiple-Valued Logic 1 (2013) 170-175.
[6] R. Faghih Mirzaee, K. Navi, Optimized adder cells for ternary ripple-carry addition, ICICE Trans. Inf. Syst. E97-D(9 (2014) 2312-2319.
[7] R. Faghih Mirzaee, K. Navi, N. Bagherzadeh, High-efficient circuits for ternary addition, VLSI Des. 2014 (2014) 1-15.
[8] S. Rezaie, R. Faghih Mirzaee, K. Navi, O. Hashemipour, From static ternary adders to high-performance race-free dynamic ones, J. Eng. 5 (2015) 1-12.
[9] CNFET Compact Model, https://nano.standard.edu/Stanford-cnfet-model (Accessed on: 10.05.2018)
[10] Predictive Technology Model (PTM), http://ptm.asu.edu (Accessed on: 10.05.2018).

https://doi.org/10.30799/jnst.187.18040530

Cite this Article as: Gudala Konica, Sreenivasulu Mamilla, Design and analysis of CMOS and CNTFET based ternary operators for scrambling, J. Nanosci. Tech. 4(5) (2018) 575–579.